MVME420/D1
MICROSYSTEMS

I/O modules

MVME420

SASI Adapter Module User's Manual

MOTOROLA

MVME420/D1

JANUARY 1983

MVME420

SASI ADAPTER MODULE

USER'S MANUAL

First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation and installation instructions, operating instructions, functional description, and support information for the MVME420 SASI Adapter Module (referred to as SAM throughout this manual). The SAM is shown in Figure 1-1.

1.2 FEATURES

Features of the SAM are listed below.

- Single-wide VME board form factor.
- Motorola I/O Channel interface compatible.
- SA1400 Shugart Associates (SASI bus) interface compatible.
- Appears as eight 1-byte read/write registers on I/O Channel address map.
- Base address configurable to one of 16 sets of 8-byte address blocks.
- Status flag register included for polling mode operation.
- Diagnostic read and write provided to verify I/O Channel data path.
- FAIL LED indicator.
- Maskable interrupt provided with strapping options to one of three I/O Channel interrupt priority levels.

1.3 SPECIFICATIONS

General specifications for the SAM are given in Table 1-1.

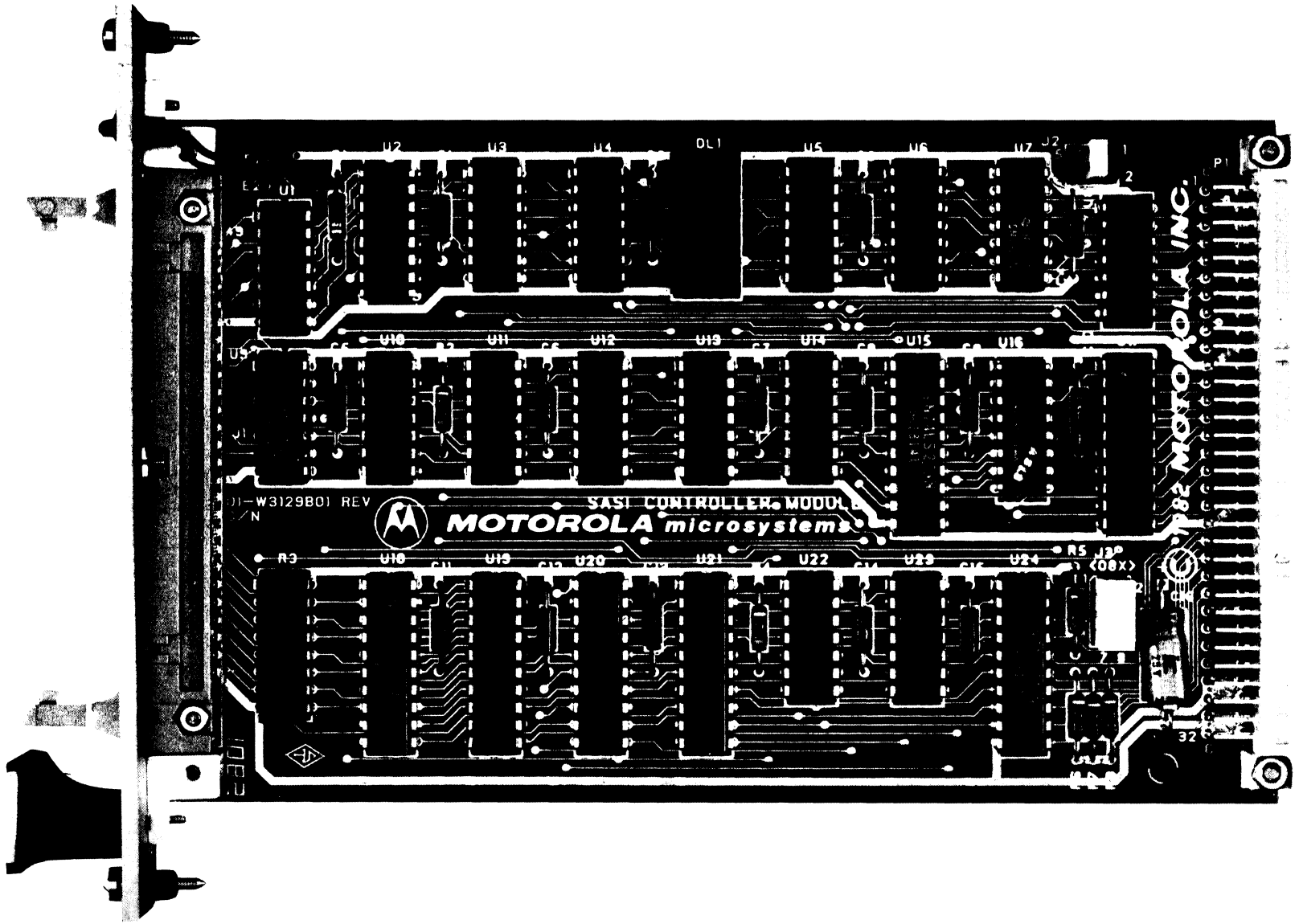


FIGURE 1-1. SASI Adapter Module

TABLE 1-1. SAM Specifications

CHARACTERISTIC	SPECIFICATIONS
Power requirements	+5 Vdc @ 1.0 A maximum
Temperature	
Operating	0° to 70° C
Storage	-40° to 85° C
Relative humidity	0 to 90% (non-condensing)
Physical characteristics	
Single-wide VME board	
PC board only	
Height	6.30 in. (160 mm)
Depth	3.94 in. (100 mm)
Thickness	0.59 in. (15 mm)
PC board with connectors and board stiffener	
Height	7.40 in. (188 mm)
Depth	5.12 in. (130 mm)
Thicknesss	0.83 in. (21 mm)

1.4 GENERAL DESCRIPTION

The SAM is an I/O Channel-compatible disk drive controller interface module, fitting the single-wide VME board form factor and connecting to the I/O Channel with a 64-pin DIN standard connector. SAM is used to expand the resources of an I/O Channel master to include a disk drive controller. SAM provides interface between the I/O Channel and the Shugart Associates SASI bus. The SASI bus is connected to a Shugart Associates SA1403D controller. SAM also provides a front panel FAIL LED indicator to indicate a module malfunction.

The user must provide a connector-compatible I/O Channel backplane or ribbon cable to connect the SAM to the I/O Channel master. Refer to the I/O Channel Specification Manual, Motorola publication number M68RIOCS, for interfacing and backplane information. The user must also provide the compatible cables to connect the SAM (via front panel connector) to the SASI disk drive device.

1.5 RELATED DOCUMENTATION

The following publications are applicable to the SAM:

- M68RIOCS I/O Channel Specification Manual
- OEM Manual Shugart Associates SA1403D Controller

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the SASI Adapter Module.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of SAM prior to system installation. The SAM has been factory tested for system operation, and is shipped with factory-installed jumpers. These factory-installed jumper connections should be verified to ensure that the module is properly configured for system operation. The SAM is configured to interface with a Shugart Associates SA1403D disk drive controller.

There are two headers on the SAM, as shown in Figure 2-1. They are J2 and J3. Table 2-1 lists each header, its function, and factory-installed jumper configuration.

TABLE 2-1. SAM Headers

HEADER NUMBER	FUNCTION	FACTORY CONFIGURATION
J2	Interrupt select	5-6
J3	Address decode	1-2, 3-4, 5-6, 7-8

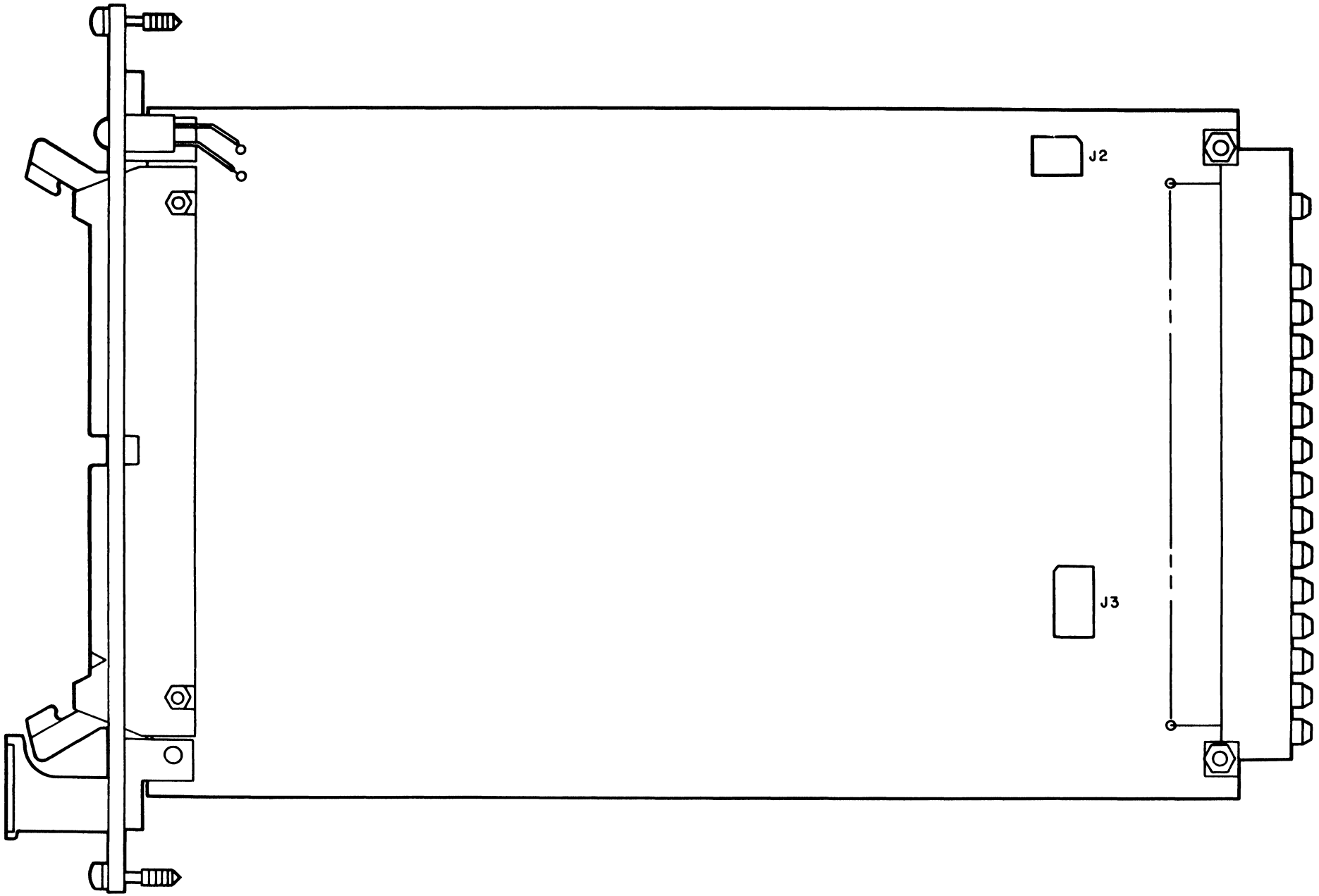


FIGURE 2-1. SAM Header Location Diagram

2.3.1 Interrupt Select Header (J2)

Header J2 controls selection of one of the three I/O Channel interrupts which the SAM can generate. The selected interrupt is generated when a request is received from the controller. Figure 2-2 illustrates the factory configuration of header J2. Table 2-2 lists the jumper configurations that determine which interrupt is selected.

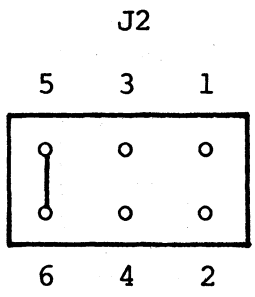


FIGURE 2-2. Interrupt Select Header (J2)

TABLE 2-2. Header J2 Configurations

PINS CONNECTED	REMARKS
1-2	Interrupt INT3* is selected.
3-4	Interrupt INT2* is selected.
5-6 (1)	Interrupt INT1* is selected.

NOTE: (1) Factory-installed jumper placement.

2.3.2 Address Decode Header (J3)

Header J3 controls selection of one of 16 blocks of eight I/O Channel addresses. Figure 2-3 illustrates the factory configuration of these headers. Table 2-3 lists the jumper configurations that determine which block of eight I/O Channel addresses is selected.

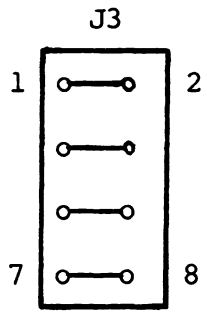


FIGURE 2-3. Address Decode Header (J3)

TABLE 2-3. Header J3 Configurations

PINS CONNECTED	REMARKS
1-2, 3-4, 5-6, 7-8 (1)	Select block 0 addresses 000-007
1-2, 3-4, 5-6	Select block 1 addresses 008-00F
1-2, 3-4, 7-8	Select block 2 addresses 010-017
1-2, 3-4	Select block 3 addresses 018-01F
1-2, 5-6, 7-8	Select block 4 addresses 020-027
1-2, 5-6	Select block 5 addresses 028-02F
1-2, 7-8	Select block 6 addresses 030-037
1-2	Select block 7 addresses 038-03F
3-4, 5-6, 7-8	Select block 8 addresses 040-047
3-4, 5-6	Select block 9 addresses 048-04F
3-4, 7-8	Select block 10 addresses 050-057
3-4	Select block 11 addresses 058-05F
5-6, 7-8	Select block 12 addresses 060-067
5-6	Select block 13 addresses 068-06F
7-8	Select block 14 addresses 070-077
none	Select block 15 addresses 078-07F

NOTE: (1) Factory-installed jumper placement.

2.4 INSTALLATION INSTRUCTIONS

This section describes how to install a SAM into a VME chassis or a 5-slot I/Omodule card cage. A typical configuration is shown in Figure 2-4. Before making any connections, ensure all power has been removed from the VME chassis or 5-slot I/Omodule card cage.

CAUTION

INSERTING/REMOVING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO MODULE COMPONENTS.

2.4.1 VME Chassis

Install a SAM into a VME chassis by performing the instructions in the following paragraphs.

2.4.1.1 I/O Channel Connection. Insert the SAM vertically from the front of the chassis. Ensure that male connector P1 mates to the fixed DIN 41612 triple-row, female, 64-pin connector. Polarity is controlled by the connector. For further details, refer to the I/O Channel specification and applicable I/O Channel master manuals (VM02 or MVME110).

2.4.1.2 Peripheral Connection. Peripheral connection to the SAM is accomplished by mating a double-row, 50-pin, female ribbon connector (such as a 3M 3425-5000) to male connector J1, as shown in Figure 2-4. Printer cable assembly, Motorola part number M68KVMPRTCE, can be used. Connect the other end of the SASI ribbon cable to the SA1403D controller.

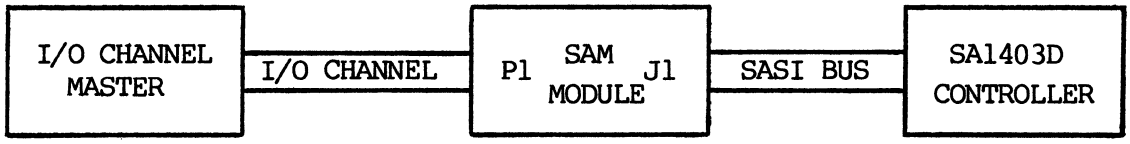


FIGURE 2-4. Typical SAM Interface Cabling Diagram

NOTE

The SA1403D controller has a factory-installed parity enable jumper (W1-A to W1-B). This jumper must be removed and re-configured (W1-B to W1-C) because the SAM does not support the parity function on the SA1403D controller.

2.4.2 5-Slot I/Omodule Card Cage

Install a SAM into a 5-slot I/Omodule card cage, which is mounted at the rear of a VM chassis, by performing the instructions in the following paragraphs.

2.4.2.1 I/O Channel Connection. Insert the SAM horizontally from the rear of the VM chassis. Ensure that male connector P1 mates to the fixed DIN 41612 triple-row, female, 64-pin connector. Polarity is controlled by the connector.

2.4.2.2 Peripheral Connection. See paragraph 2.4.1.2.

This completes connecting the SAM into a typical system. Proceed to Chapter 3.

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to initialize and operate the SASI Adapter Module in a typical system.

3.2 INDICATOR

The SAM contains one indicator -- a front panel red FAIL LED. The FAIL LED is illuminated upon reset, or can be turned on and off under software control.

3.3 OPERATING PROCEDURE

Following is a typical procedure showing how to use the SAM interface with an SA1403D controller.

a. Apply power to the system equipment.

b. Figure 3-1 is a typical disk drive routine that can be used to drive the controller.

```
MOTOROLA M68000 ASM VERSION  1.20 CRT1:  16.        .SASIWT  .SA 08/12/82 14:02:17

                        *         THIS SIMPLE EXAMPLE OF WRITING DATA TO
                        *         THE DISK USES A MOTOROLA VERSAMODULE 02
                        *         AS THE I/O CHANNEL MASTER AND ILLUSTRATES
                        *         THE TRANSFER TECHNIQUE OF "HANGING THE BUS".
                        *
                        *         THE PROGRAM FLOW IS AS FOLLOWS:
                        *           1. SELECT THE CONTROLLER
                        *           2. WAIT FOR CONTROLLER TO REQUEST A COMMAND
                        *           3. PASS A WRITE DATA COMMAND
                        *           4. WAIT FOR CONTROLER REQUEST FOR DATA
                        *           5. PASS A 256 BYTE SECTOR OF DATA
                        *           6. WAIT FOR CONTROLLER READ STATUS REQUEST.
                        *           7. READ STATUS AND MESSAGE BYTES
                        *           8. EXIT
                        *         EACH OF THE WAIT SEQUENCES WILL TIME OUT AFTER
                        *         A DELAY DOWNCOUNT AND RETURN WITH THE PROGRAM
                        *         SEQUENCE IN LOCATION STATCODE AS SSXXXXXX WHERE
                        *         X=DON'T CARE AND S=SEQUENCE CODE. SEQUENCE CODES
                        *         ARE AS FOLLOWS:
                        *           00=OK-EXAMPLE COMPLETE
                        *           10=SELECT
                        *           20=PASS COMMAND
                        *           30=PASS DATA
                        *           40=STATUS/MESSAGE
                        *           50=STATUS NOT ZERO ERROR
                        *           60=FLAG NOT ZERO ERROR
                        *           70=BUS TIMEOUT

                        * USE THE VERSABUG "MM"COMMAND UPON RETURN TO EXAMINE
                        * THE CONTENTS OF "STATCODE" LOCATION.

                        * SAM REGISTER OFFSETS FROM BASE ADDRESS OF SAM.
00000000    SEL         EQU       0
00000000    FLAG        EQU       0
00000002    COMMAND     EQU       2
00000002    STATUS      EQU       2
00000008    DATA        EQU       8

                        * SAM FLAG REGISTER MODE VALUES
00000081    BSY.CMD     EQU       $81                 CONTROLLER BUSY-COMMAND REQUEST
00000082    BSY.DATA    EQU       $82                 CONTROLLER BUSY-WRITE DATA REQUEST
00000088    BSY.STAT    EQU       $88                 CONTROLLER BUSY-READ STATUS REQUEST
00F00004    VERSABUG    EQU       $F00004             VERSABUG VECTOR
```

FIGURE 3-1. Typical Disk Drive Routine (Sheet 1 of 4)

```
45                                  * COMMAND DESCRIPTOR BLOCK(CDB) FOR A WRITE TO THE DISK SEQUENCE.
46              00003000            WRITE   ORG     $3000
47   00003000   0A00                WRITE   DC.W    $0A00                   CMD CLASS,OPCODE,LUN#
48   00003002   1000                WRITES  DC.W    $1000                   STARTING LOGICAL SECTOR#
49   00003004   0100                SECCNT  DC.W    $0100                   #SECTORS,INTERLEAVE,CONTROL FIELD
50   00003006   0100                SECTSZ  DC.W    $0100                   # BYTES/SECTOR
51   00003008   00F80001            BASE    DC.L    $00F80001               BASE ADDRESS OF SAM
52   0000300C   00003100            WTDATA  DC.L    $00003100               STARTING ADDR OF WRITE DATA
53                                  * END OF COMMAND DESCRIPTOR BLOCK
54
55   00003010   00000004            STATCODE DS.L   1                       STATUS OF WRITE OPERATION UPON EXIT
56
57                                  * START OF MAIN ROUTINE.
58              00003100            START   ORG     $3100
59   00003100   2A3C00030000        START   MOVE.L  #$30000,D5              DELAY COUNT FOR RESET
60   00003106   4E70                        RESET                           TOGGLE I/O RESET LINE
61   00003108   5385                RES     SUB.L   #1,D5
62   0000310A   66FC                        BNE.S   RES
63   0000310C   2E7C00002000              MOVE.L  #$2000,A7                 INIT STACK POINTER
64   00003112   21FC0000312E          MOVE.L  #BSER,$8                    SET BUS ERROR VECTOR
                0008
65   0000311A   227C0000300C          MOVE.L  #WTDATA,A1                  POINTER TO DATA SOURCE (MEMORY)
66   00003120   4EB900003140          JSR     WTSECT                      GO WRITE TO DISK
67   00003126   2A7900F00004  EXIT    MOVE.L  VERSABUG,A5                 SECTOR HAS BEEN WRITTEN
68   0000312C   4ED5                JMP     (A5)                        RETURN TO VERSABUG
69   0000312E   2E7C00000444  BSER    MOVE.L  #$444,A7                    EXIT THE ROUTINE ON BUS ERROR
70   00003134   21FC70000000          MOVE.L  #$70000000,STATCODE         SEQUENCE #
                3010
71   0000313C   4EF83126              JMP     EXIT
72
73                                  * THIS SUBROUTINE WRITES ONE SECTOR OF DATA FROM MEMORY
74                                  * TO THE DISK THROUGH THE SAM. THIS ROUTINE ILLUSTRATES
75                                  * THE TECHNIQUE OF "HANGING THE BUS" DURING DATA TRANSFERS
76                                  * TO THE DISK CONTROLLER.
77                                  *
78                                  * ENTRY:
79                                  *       A1=START OF WRITE DATA BLOCK (MEMORY)
80                                  * EXIT:
81                                  *       "STATCODE"= RESULT OF WRITE SEQUENCE
82                                  * THE ROUTINE ASSUMES A FIXED CDB LOCATION,A FORMATTED
83                                  * SA1004 WINCHESTER DRIVE AT LUN0,AND A SA1403D CONTROLLER.
84
85   00003140   4282                WTSECT  CLR.L   D2
86   00003142   41F83000                    LEA     WRITE,A0                BASE ADDR OF CDB
87   00003146   45F83006                    LEA     WRITE+6,A2              ADDR OF LAST CONTROLLER COMMAND+1
88   0000314A   28783008                MOVE.L  BASE,A4                     BASE ADDR OF SAM
89   0000314E   32280006                MOVE.W  6(A0),D1                    BYTES/SECTOR VALUE
90   00003152   14280004                MOVE.B  4(A0),D2                    GET # OF SECTORS
91   00003156   C2C2                    MULU    D2,D1                       (BYTES/SECTOR)*(# OF SECTORS)
92
```

FIGURE 3-1. Typical Disk Drive Routine (Sheet 2 of 4)

```
 93                          * SELECT THE CONTROLLER
 94   00003158 2A3C0002FFFF          MOVE.L   #$02FFFF,D5          DELAY COUNTER
 95   0000315E 18BC0001              MOVE.B   #1,SEL(A4)           SELECT CONTROLLER
 96   00003162 0C140081      WAIT1   CMP.B    #BSY,CMD,FLAG(A4)    WAIT FOR A COMMAND REQUEST
 97   00003166 6710                  BEQ.S    PASSCMD
 98   00003168 5385                  SUB.L    #1,D5
 99   0000316A 66F6                  BNE.S    WAIT1
100   0000316C 21FC10000000          MOVE.L   #$10000000,STATCODE  SEQUENCE #
               3010
101   00003174 60000090              BRA      LEAVE
102   00003178 2A3C0003FFFF  PASSCMD  MOVE.L   #$03FFFF,D5          DELAY COUNTER
103   0000317E 19580002      CMDLP   MOVE.B   (A0)+,COMMAND(A4)    PASS A COMMAND BYTE
104   00003182 B5C8                  CMPA.L   A0,A2                LAST BYTE?
105   00003184 66F8                  BNE.S    CMDLP
106   00003186 0C140082      WAIT2   CMP.B    #BSY,DATA,FLAG(A4)   WAIT FOR A DATA REQUEST
107   0000318A 6710                  BEQ.S    PASSDATA
108   0000318C 5385                  SUB.L    #1,D5
109   0000318E 66F6                  BNE.S    WAIT2
110   00003190 21FC20000000          MOVE.L   #$20000000,STATCODE  SEQUENCE #
               3010
111   00003198 6000006C              BRA      LEAVE
112                          * IF THE SAM DETECTS A SEQUENCE ERROR DURING THE DATA TRANSFER
113                          * THE BUS WILL "HANG" AND CAUSE THE HOST TO TIME OUT WITH A
114                          * BUS ERROR EXCEPTION.
115   0000319C 21FC30000000  PASSDATA MOVE.L   #$30000000,STATCODE  SEQUENCE #
               3010
116   000031A4 2419          DATALP  MOVE.L   (A1)+,D2             FETCH DATA FROM MEMORY
117   000031A6 05CC0008              MOVEP.L  D2,DATA(A4)          WRITE DATA BLOCK TO DISK
118   000031AA 5941                  SUB.W    #4,D1                DECREMENT BYTE COUNTER
119   000031AC 66F6                  BNE.S    DATALP               LAST BYTE?
120   000031AE 2A3C0003FFFF          MOVE.L   #$03FFFF,D5          DELAY COUNTER
121   000031B4 0C140088      STAT1   CMP.B    #BSY,STAT,FLAG(A4)   WAIT FOR READ STATUS REQUEST
122   000031B8 6710                  BEQ.S    STAT2
123   000031BA 5385                  SUB.L    #1,D5
124   000031BC 66F6                  BNE.S    STAT1
125   000031BE 21FC40000000          MOVE.L   #$40000000,STATCODE  SEQUENCE #
               3010
126   000031C6 6000003E              BRA      LEAVE
127   000031CA 21FC50000000  STAT2   MOVE.L   #$50000000,STATCODE  SEQUENCE #
               3010
128   000031D2 102C0002              MOVE.B   STATUS(A4),D0        READ STATUS BYTE
129   000031D6 E148                  LSL.W    #8,D0
130   000031D8 102C0002              MOVE.B   STATUS(A4),D0        READ MESSAGE BYTE
131   000031DC 0C400000              CMP.W    #0,D0                STATUS SHOULD BE 0
132   000031E0 6702                  BEQ.S    STAT3
133   000031E2 6022                  BRA.S    LEAVE
134   000031E4 2A3C0003FFFF  STAT3   MOVE.L   #$03FFFF,D5          DELAY COUNT
135   000031EA 0C140000              CMP.B    #0,FLAG(A4)          SEQUENCE COMPLETE?
136   000031EE 670E                  BEQ.S    OK
137   000031F0 5385                  SUB.L    #1,D5
```

FIGURE 3-1. Typical Disk Drive Routine (Sheet 3 of 4)

```
138    000031F2 66F0                    BNE.S    STAT3
139    000031F4 21FC60000000            MOVE.L   #$60000000,STATCODE   SEQUENCE #
                3010
140    000031FC 6008                    BRA.S    LEAVE
141    000031FE 21FC00000000 OK         MOVE.L   #0,STATCODE
                3010
142    00003206 4E75          LEAVE     RTS
143                                     END

****** TOTAL ERRORS       0---    0
****** TOTAL WARNINGS     0---    0
```

SYMBOL TABLE LISTING

SYMBOL NAME	SECT	VALUE	SYMBOL NAME	SECT	VALUE
BASE		00003008	SECCNT		00003004
BSER		0000312E	SECTSZ		00003006
BSY.CMD		00000081	SEL		00000000
BSY.DATA		00000082	START		00003100
BSY.STAT		00000088	STAT1		000031B4
CMDLP		0000317E	STAT2		000031CA
COMMAND		00000002	STAT3		000031E4
DATA		00000008	STATCODE		00003010
DATALP		000031A4	STATUS		00000002
EXIT		00003126	VERSABUG		00F00004
FLAG		00000000	WAIT1		00003162
LEAVE		00003206	WAIT2		00003186
OK		000031FE	WRITE		00003000
PASSCMD		00003178	WRITES		00003002
PASSDATA		0000319C	WTDATA		0000300C
RES		00003108	WTSECT		00003140

FIGURE 3-1. Typical Disk Drive Routine (Sheet 4 of 4)

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides overall block diagram level descriptions for the SASI Adapter Module. A general description provides an overview of the module, followed by a detailed description of each section of the SAM.

4.2 MODULE DESCRIPTION

SAM is designed to provide an interface between the I/O Channel and a Shugart Associates SA1403D disk drive controller via the SASI bus. SAM supports a single host, non-arbitrating, no parity implementation of the SASI bus.

A block diagram of the SAM is provided in Figure 4-1. SAM provides complete buffering of all I/O Channel and SASI bus address, data, and control lines. The I/O Channel address and control lines are used to decode the register or function accessed by the host. This host function is compared to the current SASI bus state, and the appropriate function acknowledgement is either returned to the host or withheld due to an exception condition being detected. Functions such as a read or write to/from the diagnostic register are independent of the SASI bus state and are completed and acknowedged by the SAM.

Some of the I/O Channel "register" addresses are functions that do not require an actual register. An example of this is the command "register". When writing to the command register, the function is decoded and the command byte is passed through the SAM data buffers to the controller.

The interrupt logic combines the interrupt enable bit from the control register and the request from the controller to issue an I/O Channel interrupt on the selected level.

SAM supports the select, command, data, transfer, and status sequences, as described in the Shugart Associates SA14030 controller OEM manual. For this implementation, SAM contains the following registers: control, status, flag, diagnostic read/write, command, select, and data read/write. These registers are defined in Table 4-1 and the explanations that follow.

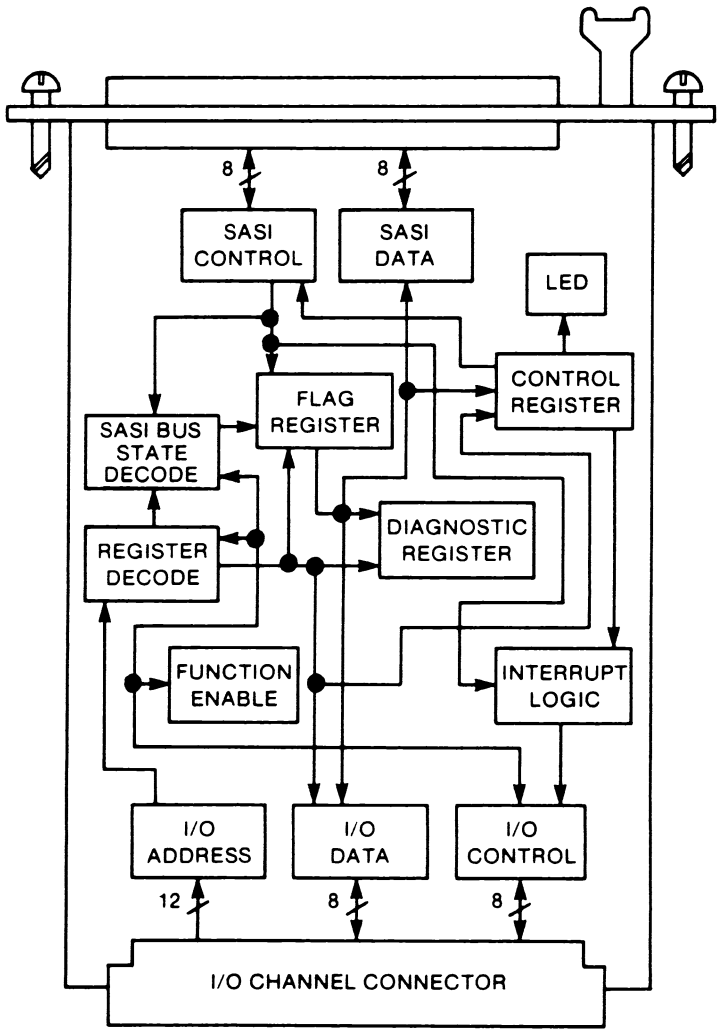


FIGURE 4-1. SAM Functional Block Diagram

TABLE 4-1. SAM Registers

REGISTER	OFFSET (1)	R/W	FUNCTION
SELECT	0	W	SA1400 select sequence
FLAG	0	R	SAM status
COMMAND	1	W	SA1400 command sequence
STATUS	1	R	SA1400 status sequence
DIAGWRT	2	W	SAM diagnostic register
DIAGRD	2	R	SAM diagnostic register
CTRL	3	W	SAM control register
DATA	4-7 (2)	R/W	SA1400 data sequence

NOTES:

(1) Base address is Nx8 where N has range of 0-15 defined by the jumper placement on header J1.

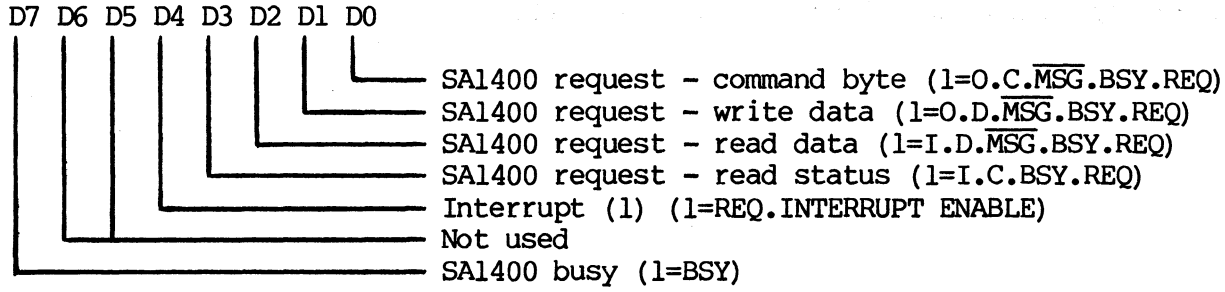
(2) Data register is mapped redundantly from offset 4-7. This mapping scheme allows use of the MC68000 MOVEP instruction to pass multiple bytes between host and controller with a single instruction.

4.2.1 Select Register

Writing a $01 to this register selects the controller. This must precede any command sequence and is valid only if the controller is not currently selected.

4.2.2 Flag Register

This register contains status information about the SAM and SASI bus state. The bit definition is:



NOTE: (1) Interrupt = (interrupts enabled and SA1400 request)

4.2.3 Command Register

A series of writes to this register constitutes a command transfer sequence as described in the SA1403D Controller OEM Manual.

4.2.4 Status Register

A 2-byte read from this register completes the status and message transfer sequence for the SA1403D controller. The first byte is the status byte (refer to the SA1403D Controller OEM Manual for definitions) and the second byte is $00. Both bytes must be read to complete the transfer sequence.

4.2.5 Diagnostic Write Register

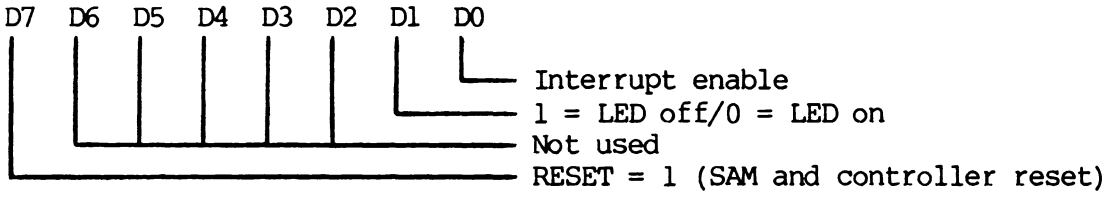
This is a write-only register used for I/O Channel data path verification. The contents of this register may be read from the diagnostic read register.

4.2.6 Diagnostic Read Register

This is a read-only register used in conjunction with the diagnostic write register.

4.2.7 Control Register

This is a write-only control register for the SAM. The bit definition is:



4.2.8 Data Register

The data register is used to read data and sense information from the controller, and to write data to the controller.

4.3 FUNCTIONAL OPERATION

The SAM may be in any one of five possible states as reflected by the flag register.

a. Not selected ---------- Flag bit 7 = 0
b. Request, command byte -------- Flag bit 0 = 1 and bit 7 = 1
c. Request, write data ---------- Flag bit 1 = 1 and bit 7 = 1
d. Request, read data ---------- Flag bit 2 = 1 and bit 7 = 1
e. Request, read status --------- Flag bit 3 = 1 and bit 7 = 1

After the SAM has been selected, the host must respond to the SAM-generated request with a read or write to the appropriate SAM register(s) (i.e., command, status, or data). The SAM flag, diagnostic write, diagnostic read, and control registers may be accessed at any time without regard to the current state of the SASI bus. The sequence and format of each of the five states is specified in the SA1403D Controller OEM Manual.

The request from the selected controller may be detected by any combination of the following schemes:

a. Polling - Read the flag register until a request is detected (i.e., SA1400 busy, flag bit 7 = 1).

b. Interrupt - With interrupts enabled (control bit 0 = 1), an I/O Channel interrupt (INT1*-INT3*) will be generated when the controller enters the request sequence.

c. Hanging the bus - During any of the SA1403D controller sequences, the controller will deactivate and reactivate the request for each sequential byte transferred between the host and the controller. This requesting sequence is useful when the host is writing command blocks, reading status, and reading or writing data when the first byte is available for transfer. Therefore, because the actual transfer by the controller occurs only at each request, the next sequential byte to be transferred to/from the SAM could be written/read by the host prior to the next controller request being activated.

4.3.1 Operation Sequence

The transfer rate between the host and the controller will depend on the controller being used. The SA1403D controller has a 256-byte data buffer and accepts command bytes or data bytes at approximately 3.6 usec/byte.

The typical host sequence for a disk operation is:

a. Select the controller (write $01 to select register).

b. Transfer the command descriptor block to the controller (SAM command register).

c. Transfer data block(s) (256 bytes/block to/from the SAM data register).

d. Read operation status (two bytes from the SAM status register).

The format of the command descriptor blocks and status codes are defined in the SA1403D Controller OEM Manual.

4.3.2 Sequence Error Detection

SAM detects only one exception condition -- a sequence error. A sequence error occurs when the host attempts to access a register not used in the function requested by the controller (i.e., reading the data register during a command request by the controller). The SAM flag, control, diagnostic write/diagnostic read registers can be accessed at any time, regardless of the current controller state, without causing an exception to occur. When an exception does occur, the SAM will not respond to the invalid access, and the host will be left to time out.

4.4 DETAILED DESCRIPTION

Refer to the schematic diagram during the following explanation.

Whenever the host accesses the SAM, the address/register decoder logic of U15, U16, and U17 will cause one of the outputs of U15 or U23A to be true upon receipt of a valid STB* signal from the host. These function outputs control the selection of the controller, source, or destination of data within the SAM, and the I/O Channel interface control lines.

The SASI bus state decoder (U2) outputs reflect the current SASI bus function being performed. These outputs can be read by the host from the flag read register (U20). The SASI bus state outputs are also compared to I/O Channel decoder outputs at U14 to ensure that the host is accessing the register requested by the controller. The result of this comparison will determine if XACK* is returned to the host or if the host will be left to time out. Access of the diagnostic (U21), control (U22 and U23B), or flag read (U20) registers is independent of the current SASI bus state and, therefore, is not a function of the U14 comparison. Whenever the host performs the requested function, the -ACK signal is asserted to the controller. The controller then removes the -REQ signal to complete the sequence.

Write-only control register bits are used to enable interrupts (D0), light the FAIL LED (D1), and software reset the controller and SAM (D7). The other bits in the control register have no function.

Reset logic (U12) provides the controller with a required single pulse each time a hardware or software reset is received.

The 8-bit, bidirectional data bus is buffered from the I/O Channel by U24 and from the SASI bus by U18 and U19.

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector signal descriptions , parts list and associated parts location diagram, and a schematic diagram for the SASI Adapter Module.

5.2 CONNECTOR SIGNAL DESCRIPTIONS

The SAM has two interface connectors -- one to connect it to the I/O Channel and one to connect it to the SA1403D controller.

5.2.1 I/O Channel Connector

Connector P1 on the SAM is a standard DIN 41612 triple-row, 64-pin, male connector. The backplane/ribbon cable uses the female connector. Table 5-1 lists the connector P1 pin assignments. Additional information can be found in the I/O Channel Specification Manual.

5.2.2 Peripheral Connector

Peripheral connector J1 on the SAM is a double-row, 50-pin, male connector, mating to a female ribbon connector such as a 3M 3425-5000. Table 5-2 lists the connector J1 pin assignments.

5.3 PARTS LIST

Table 5-3 lists the components of the SAM. This list reflects the latest issue of SAM hardware at the time of printing. A parts location diagram is provided in Figure 5-1.

5.4 DIAGRAMS

Figure 5-2 is the schematic diagram of the SAM.

TABLE 5-1. I/O Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A10, A17-A19, A24,A25, A31,A32, C11,C20, C25,C31, C32	GND	GROUND
A11	A11	ADDRESS bus (bit 11) - One of 11 input signals used to selectively access the SAM.
A12	A10	ADDRESS bus (bit 10) - Same as A11 on pin A11.
A13	A8	ADDRESS bus (bit 8) - Same as A11 on pin A11.
A14	A6	ADDRESS bus (bit 6) - Same as A11 on pin A11.
A15	A4	ADDRESS bus (bit 4) - Same as A11 on pin A11.
A16	A2	ADDRESS bus (bit 2) - Same as A11 on pin A11.
A20	D7	DATA bus (bit 7) - Bidirectional signal used to transmit data between the I/O Channel master and the SAM.
A21	D6	DATA bus (bit 6) - Same as D7 on pin A20.
A22	D4	DATA bus (bit 4) - Same as D7 on pin A20.
A23	D2	DATA bus (bit 2) - Same as D7 on pin A20.
A26,C26	-12V	-12 Vdc Power - Not used.
A27, C8-C10, C27	(Reserved)	N/A
A28,C28	+12V	+12 Vdc Power - Not used.
A29,A30, C29,C30	+5V	+5 Vdc Power - Used by the module logic circuits.
C1	INT4*	INTERRUPT REQUEST 4 - Not used.
C2	INT3*	INTERRUPT REQUEST 3 - One of three active low output signal lines used by the SAM to interrupt the I/O Channel master.
C3	INT2*	INTERRUPT REQUEST 2 - Same as INT3* on pin C2.
C4	INT1*	INTERRUPT REQUEST 1 - Same as INT3* on pin C2.

TABLE 5-1. I/O Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C5	IORES*	INPUT/OUTPUT RESET - Active low input signal used to reset the SAM.
C6	XACK*	TRANSMIT ACKNOWLEDGE - Active low output signal used to advise the I/O Channel master that write data is latched and read data is available.
C7	CLK	CLOCK - Free-running input signal used by the SAM for internal synchronization and timing.
C12	A9	ADDRESS bus (bit 9) - Same as A11 on pin A11.
C13	A7	ADDRESS bus (bit 7) - Same as A11 on pin A11.
C14	A5	ADDRESS bus (bit 5) - Same as A11 on pin A11.
C15	A3	ADDRESS bus (bit 3) - Same as A11 on pin A11.
C16	A1	ADDRESS bus (bit 1) - Same as A11 on pin A11.
C17	A0	ADDRESS bus (bit 0) - Same as A11 on pin A11.
C18	STB*	STROBE - An input signal. A high to low transition starts the I/O Channel cycle. A low to high transition ends the cycle.
C19	WT*	WRITE - An input signal that is low when the I/O Channel is in the write cycle, and high when the I/O Channel is in the read cycle.
C21	D5	DATA bus (bit 5) - Same as D7 on pin A20.
C22	D3	DATA bus (bit 3) - Same as D7 on pin A20.
C23	D1	DATA bus (bit 1) - Same as D7 on pin A20.
C24	D0	DATA bus (bit 0) - Same as D7 on pin A20

NOTE: When a 50-pin ribbon cable is used, the 14 power lines (A27-A32 and C27-C32) are not connected by the cable. Power to the device interfacing with the I/O Channel must be supplied by alternate means.

TABLE 5-2. Peripheral Connector J1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-49 (odd numbers)	GND	GROUND
2	-DB0	DATA BIT 0 - Bidirectional data lines used to transfer 8-bit parallel data to/from the host adapter. Negative logic is used and bit 7 is the MSB.
4	-DB1	DATA BIT 1 - Same as DB0 on pin 2.
6	-DB2	DATA BIT 2 - Same as DB0 on pin 2.
8	-DB3	DATA BIT 3 - Same as DB0 on pin 2.
10	-DB4	DATA BIT 4 - Same as DB0 on pin 2.
12	-DB5	DATA BIT 5 - Same as DB0 on pin 2.
14	-DB6	DATA BIT 6 - Same as DB0 on pin 2.
16	-DB7	DATA BIT 7 - Same as DB0 on pin 2.
18	(Reserved)	Not used.
20-34 (even numbers)	(Reserved)	Not used.
36	-BSY	BUSY - Made true in response to the SEL line from the host adapter to indicate that the host bus is currently in use.
38	-ACK	ACKNOWLEDGE - Made true in response to each true REQ signal from the controller.
40	-RST	RESET - When made true by the host, the controller goes to an idle condition.
42	-MSG	MESSAGE - When true, indicates that the command is completed and status has been transferred.
44	-SEL	SELECT - When made true, indicates the beginning of the command transaction.
46	-C/D	CONTROL/DATA - When true, the data transmitted will be command or status bytes; when false, the data will be disk data bytes.

TABLE 5-2. Peripheral Connector J1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
48	-REQ	REQUEST - When true and I/O is true, data on the host bus is driven by the controller. When true and I/O is false, data is driven by the host adapter.
50	-I/O	INPUT/OUTPUT - When true, data on the bus is driven by the controller; when false, data is driven by the host adapter.

NOTE: A negative sign that precedes a signal mnemonic denotes an active low signal.

TABLE 5-3. SAM Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8129B01	Printed wiring board, SAM
C1-C15	21SW992C025	Capacitor, ceramic, .1 uF @ 50 Vdc
C16	23NW9618A33	Capacitor, electrolytic, 22 uF @ 25 Vdc
DL1	01NW9804C13	Delay line, triple, 100 nsec
E1, E2	48NW9612A34	Indicator light, red, 5 Vdc
J1	28NW9802D76	Connector, right angle, 50-position slider
J2	28NW9802B21	Header, double-row post, 6-pin
J3	28NW9802C43	Header, double-row post, 8-pin
P1	28NW9802E05	Connector, 64-pin plug
R1	06SW-124A33	Resistor, fixed, film, 220 ohm, 5%, 1/4 W
R2, R4-R8	06SW-124A65	Resistor, fixed, film, 4.7k ohm, 5%, 1/4 W
R3	51NW9626A20	Resistor network, 220/330 ohm
U1,U5	51NW9615E93	I.C. SN74LS14N
U2	51NW9615C69	I.C. SN74LS138N

TABLE 5-3. SAM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U3	51NW9615C21	I.C. SN74LS04N
U4	51NW9615F05	I.C. SN74LS20N
U6	51NW9615E77	I.C. SN74LS27N
U7,U9	51NW9615A42	I.C. MC7438P
U8,U13	51NW9615C22	I.C. SN74LS08N
U10	51NW9615E91	I.C. SN74LS00N
U11,U22,U23	51NW9615C25	I.C. SN74LS74N
U12	51NW9615F41	I.C. DM74LS164N
U14	51NW9615F06	I.C. SN74LS51N
U15	51NW9615F52	I.C. SN74LS273N
U16	51NW9615H72	I.C. SN74LS259N
U17	51NW9615H01	I.C. AM25LS2521PC
U18	51NW9615E95	I.C. SN74LS240N
U19	51NW9615F79	I.C. SN74S240N
U20	51NW9615F02	I.C. 74LS244N
U21	51NW9615E99	I.C. SN74LS374N
U24	51NW9615E96	I.C. SN74LS245
	02SW990D007	Nut, hex, M 2 x 0.4 x 1.6
	03SW993D110	Screw, phillips, M 2 x 0.4 x 10
	03SW993D206	Screw, phillips, M 2.5 x 0.45 x 6
	07-W4252B01	Bracket, card mounting
	29NW9805B17	Jumper, shorting insulated (use at J2, 5-6; J3, 1-2, 3-4, 5-6, 7-8)
	33-W4365B01	I/O module
	43NW9002A98	Coding bar, M DIN connector
	64-W4255B01	Front panel, RS-232C I/O

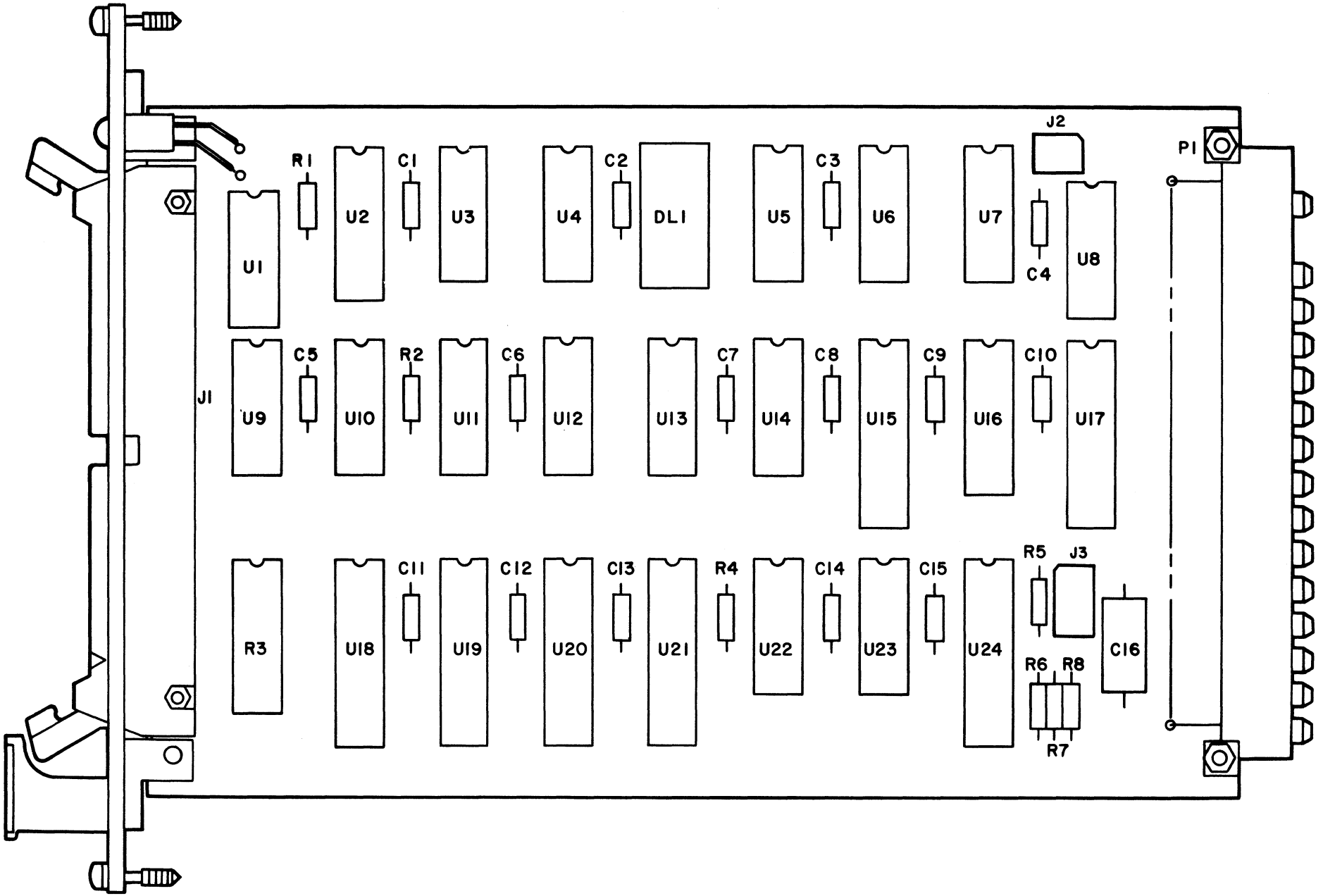


FIGURE 5-1. SAM Parts Location Diagram

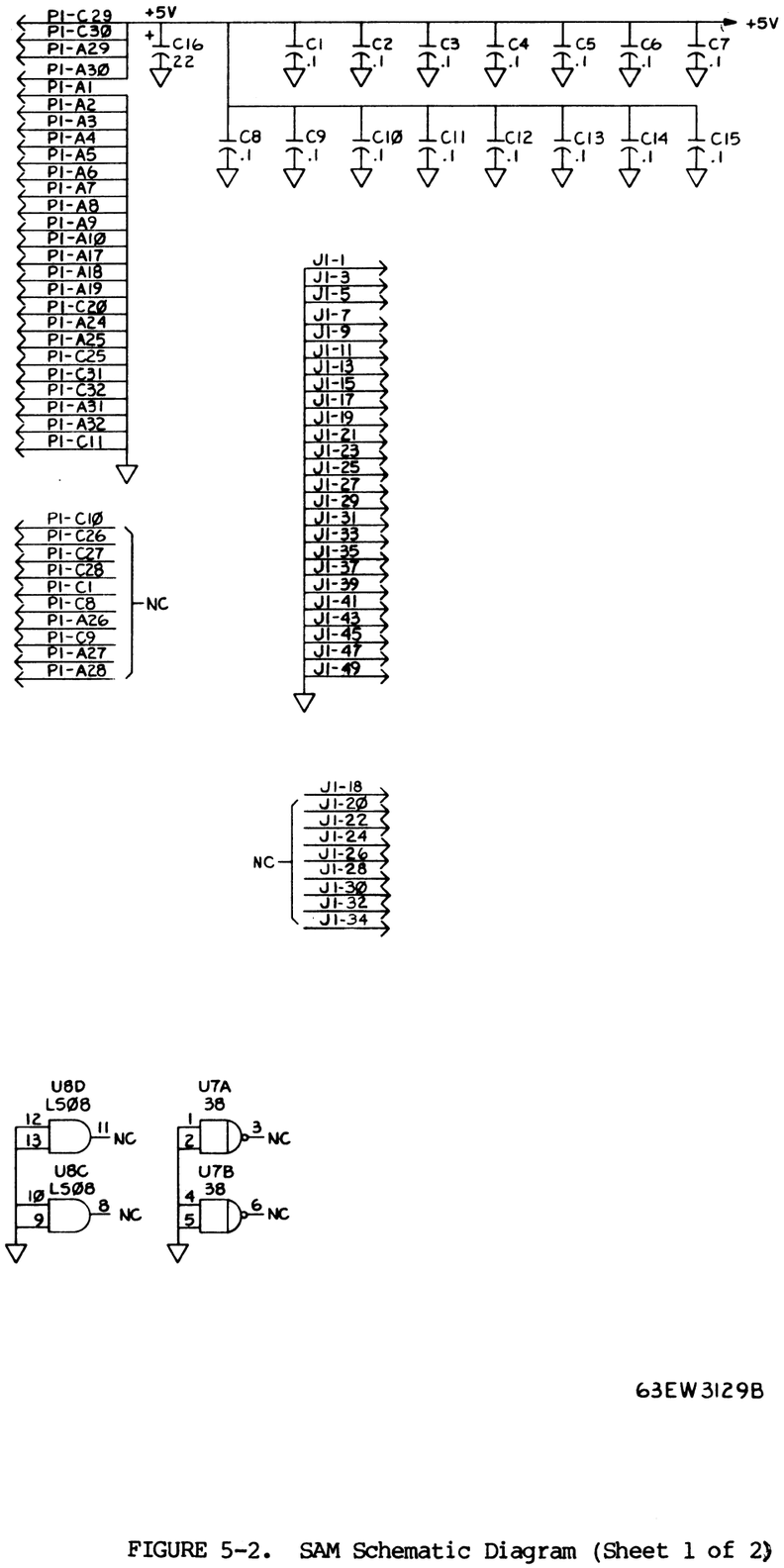
NOTES:

1. FOR REFERENCE DRAWING REFER TO BILL OF MATERIAL Ø1-W3129B.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISIONS.
6. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE I.

6 TABLE I

REF DES	TYPE 4	GND	+5V
U1	74LS14	7	14
U2	74LS138	8	16
U3	74LS04	7	14
U4	74LS20	7	14
U5	74LS14	7	14
U6	74LS27	7	14
U7	7438	7	14
U8	74LS08	7	14
U9	7438	7	14
U10	74LS00	7	14
U11	74LS74	7	14
U12	74LS164	7	14
U13	74LS08	7	14
U14	74LS51	7	14
U15	74LS273	10	20
U16	74LS259	8	16
U17	74LS688	10	20
U18	74LS240	10	20
U19	745240	10	20
U20	74LS244	10	20
U21	74LS374	10	20
U22	74LS74	7	14
U23	74LS74	7	14
U24	74LS245	10	20
DL1	(100 NS)	7	14

U24	
R8	
P1	
J3	
DL1	
C16	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	



63EW3129B REV B SH 1 OF 2

FIGURE 5-2. SAM Schematic Diagram (Sheet 1 of 2)

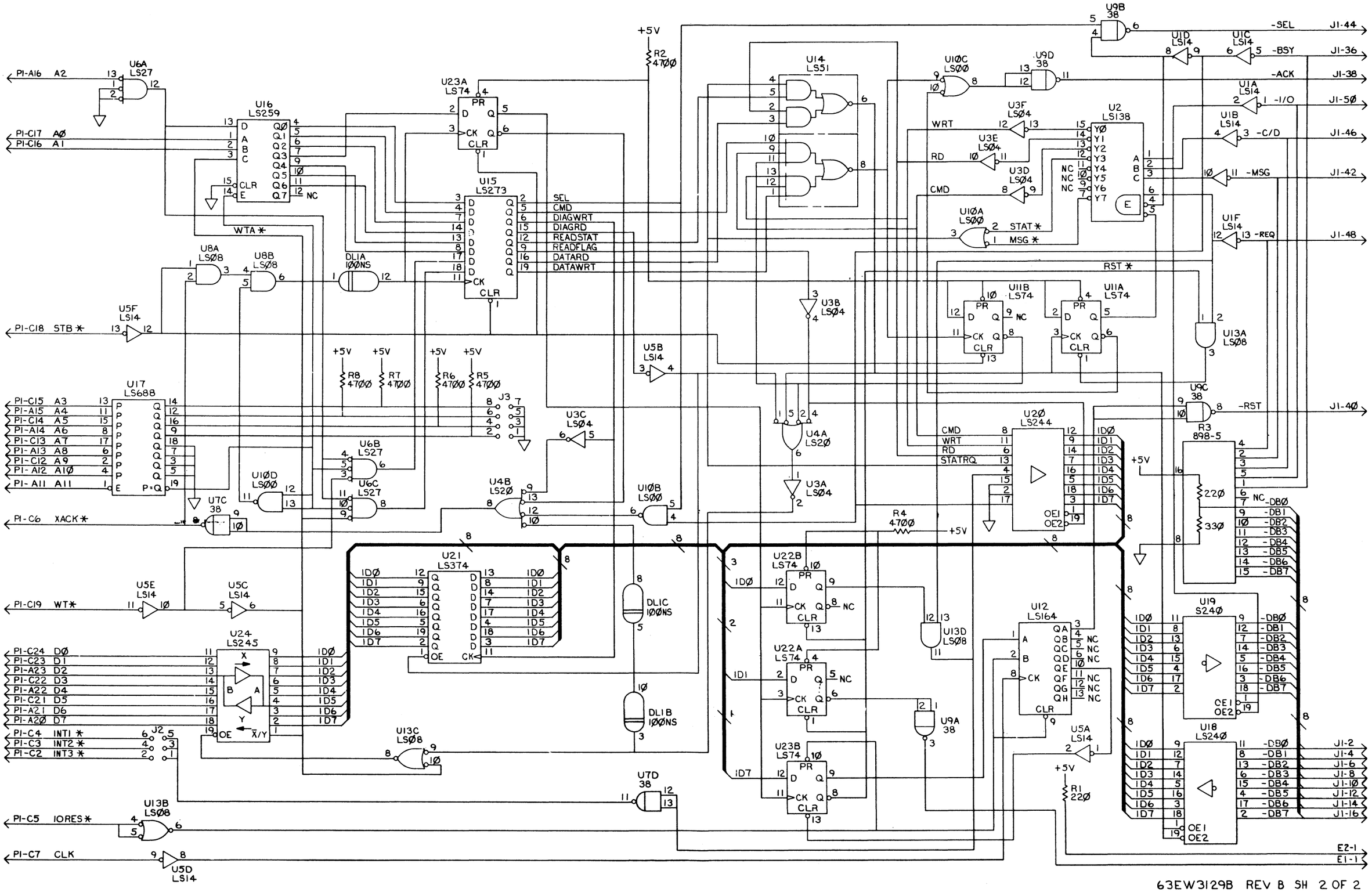


FIGURE 5-2. SAM Schematic Diagram (Sheet 2 of 2) 5-11/5-12

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